# TSC7650A
# Chopper-Stabilized Operational Amplifier
## • Low Offset Voltage 5 μV Max.
## • Low Supply Current 1.7 mA

## General Description

The TSC7650A CMOS chopper-stabilized operational amplifier practically removes offset voltage error terms from system error calculations. The 5 μV maximum $V_{OS}$ specification, for example, represents a fifteen times improvement over the industry standard OP07E. The 0.2 μV/°C Max. offset drift specification is six times lower than the OP07E. The increased performance eliminates $V_{OS}$ trim procedures, periodic potentiometer adjustment and the reliability problems caused by damaged trimmers. The TSC7650A features lower maximum power supply current and higher slew rate than the ICL7650. The TSC7650A power supply current is 2.5 mA maximum.

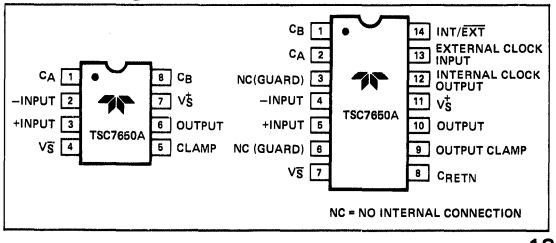
The TSC7650A performance advantages are achieved without the additional manufacturing complexity and cost incurred with laser or "zener zap" $V_{OS}$ trim techniques. The TSC7650A is one of the lowest cost precision operational amplifiers available.

The TSC7650A nulling scheme corrects both dc $V_{OS}$ errors and $V_{OS}$ drift errors with temperature. A nulling amplifier alternately corrects its own $V_{OS}$ errors and the main amplifier $V_{OS}$ error. Offset nulling voltages are stored on two user supplied external capacitors. The capacitors connect to the internal amplifier $V_{OS}$ null points. The main amplifier input signal is never switched. Switching spikes are not present at the TSC7650A output. The null scheme keeps $V_{OS}$ errors low throughout the operating temperature range. Laser and "zener zap" trimming can correct for $V_{OS}$ at only one temperature.

The nulling circuit oscillator and control circuits are integrated on chip. Only two external $V_{OS}$ error storage capacitors are required. The TSC7650A operates as a conventional operational amplifier with vastly improved input specifications. The low $V_{OS}$ and $V_{OS}$ drift errors make the TSC7650A ideal for thermocouple, thermistor, and strain gauge applications. Low dc errors and high open loop gain make the TSC7650A an excellent preamplifier for precision analog to digital converters like the TSC7135, TSC800, and TSC7109.

The 14-pin dual in line package (DIP) has an external oscillator input to drive the nulling circuitry for optimum noise performance. Both the 8 and 14-pin DIP have an output voltage clamp circuit to minimize overload recovery time.

## Pin Configuration




## Features

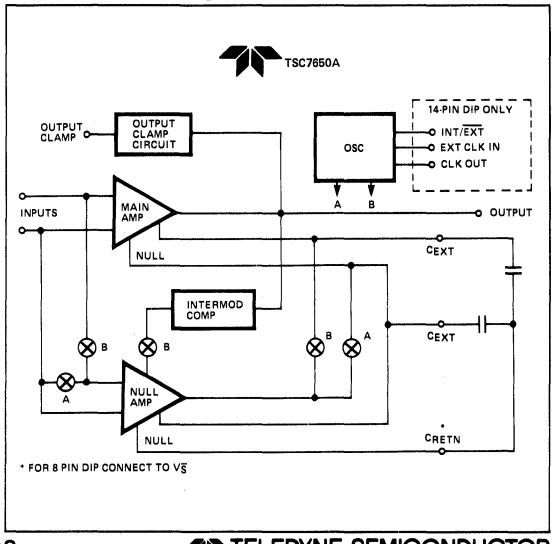
- Low Input Offset Voltage ..... 5 μV Max.
- Low Input Offset Voltage Drift ..... 0.2 μV/°C Max.
- Low Input Bias Current ..... 15 pA Max.
- High Impedance Differential CMOS Inputs ..... $10^{12}$ Ω
- High Open Loop Voltage Gain ..... 120 dB Min.
- High Slew Rate ..... 4.0 V/μs
- Low Power Operation ..... 17 mW
- Output Clamp Speeds Recovery Time
- Compensated Internally for Stable Unity Gain Operation
- Pin Compatible Replacement for ICL7650

## Ordering Information

| Part No. | Package | Temp. Range | Max. $V_{OS}$ |
|---|---|---|---|
| *TSC7650ACPA | 8-Pin Plastic Dip | 0°C to + 70°C | 5 μV |
| *TSC7650AIJA | 8-Pin CerDIP | -25°C to + 85°C | 5 μV |
| *TSC7650ACPD | 14-Pin Plastic Dip | 0°C to + 70°C | 5 μV |
| *TSC7650AIJD | 14-Pin CerDIP | -25°C to + 85°C | 5 μV |

*Available with 160 hour, +125°C burn-in. Add /BI to part number suffix.

## Functional Diagram

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# Chopper-Stabilized Operational Amplifier

- Low Offset Voltage 5 μV Max.
- Low Supply Current 1.7 mA

## Absolute Maximum Ratings

Total Supply Voltage ($V_S^+$ to $V_S^-$) ..... 18 Volts
Input Voltage ..... ($V_S^+$ + 0.3) to ($V_S^-$ - 0.3) Volts
Storage Temp. Range ..... -55°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C
Voltage on Oscillator Control Pins ..... $V_S^+$ to $V_S^-$
Output Short Circuit Duration ..... Indefinite
Current into Any Pin ..... 10 mA
While Operating (Note 4) ..... 100 μA
Operating Temp. Range
I Device ..... -25°C to +85°C
C Device ..... 0°C to +70°C
Package Power Dissipation ($T_A$ = 25°C)
CerDIP Package ..... 500 mV
Plastic Package ..... 375 mW

## Electrical Characteristics: $V_S^+$ = +5 V, $V_S^-$ = -5 V, $C_A$ = $C_B$ = 0.1 μF, $T_A$ = 25°C.

| TYPE | NO. | SYMBOL | PARAMETER | TEST CONDITIONS | TSC7650A MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| INPUT | 1 | $V_{OS}$ | Input Offset Voltage | $T_A$ = +25°C | — | ± 0.7 | ± 5.0 | μV |
| | 2 | $\frac{\Delta V_{OS}}{\Delta T}$ | Input Offset Voltage Average Temp. Coefficient | Operating Temp Range (Note 1) | — | 0.08 | 0.2 | μV/°C |
| | 3 | $I_{BIAS}$ | Input Bias Current | $T_A$ = + 25°C | — | 1.5 | 15 | pA |
| | | | | 0°C ≤ $T_A$ ≤ + 70°C | — | 35 | 150 | |
| | | | | -25°C ≤ $T_A$ ≤ + 85°C | — | 100 | 400 | |
| | 4 | $I_{OS}$ | Input Offset Current | $T_A$ = 25°C | — | 0.5 | — | pA |
| | 5 | $e_{np-p}$ | Input Noise Voltage | $R_S$ = 100 Ω 0.1 to 10 Hz | — | 4.0 | — | $\mu V_{p-p}$ |
| | 6 | $I_n$ | Input Noise Current | f = 10 Hz | — | 0.01 | — | $pA/\sqrt{Hz}$ |
| | 7 | $R_{IN}$ | Input Resistance | | — | $10^{12}$ | | Ω |
| | 8 | CMVR | Common-Mode Voltage Range | | -5.0 | -5.2 to +2.0 | +1.5 V | V |
| | 9 | CMRR | Common-Mode Rejection Ratio | CMVR = -5 V to +1. 5 V | 120 | 130 | — | dB |
| OUTPUT | 10 | $A_V$ | Large-Signal Voltage Gain | $R_L$ = 10 kΩ | 120 | 130 | — | dB |
| | 11 | $V_{OUT}$ | Output Voltage Swing (Note 3) | $R_L$ = 10 kΩ | ± 4.7 | ± 4.85 | — | V |
| | | | | $R_L$ = 100 kΩ | — | ± 4.95 | — | |
| | 12 | | Clamp ON Current (Note 2) | $R_L$ = 100 kΩ | 25 | 70 | 200 | μA |
| | 13 | | Clamp OFF Current (Note 2) | -4.0 V < $V_{OUT}$ < + 4.0 V | — | 1 | — | pA |
| DYNAMIC | 14 | $B_W$ | Unity Gain Bandwidth | Unity Gain (+1) | — | 1.0 | — | MHz |
| | 15 | $S_R$ | Slew Rate | $C_L$ = 50 pF, $R_L$ = 10 kΩ | — | 4.0 | — | V/μs |
| | 16 | $t_r$ | Rise Time | | — | 0.2 | — | μs |
| | 17 | | Overshoot | | — | 30 | — | % |
| | 18 | $f_{ch}$ | Internal Chopping Frequency | Pins 12-14 Open (DIP) | 120 | 300 | 420 | Hz |
| SUPPLY | 19 | $V_S^+$ to $V_S^-$ | Operating Supply Range | | 4.5 | — | 16 | V |
| | 20 | $I_S$ | Supply Current | No Load | — | 1.7 | 2.5 | mA |
| | 21 | PSRR | Power Supply Rejection Ratio | $V_S$ = ± 3 V to ± 8 V | 120 | 130 | — | dB |

**Notes:**

1. Operating temperature range is -25°C to +85°C for "I" grade and 0°C to +70°C for "C" grade.
2. See OUTPUT CLAMP discussion.
3. OUTPUT CLAMP not connected. See characteristic curves for output swing vs clamp current.
4. Limiting input current to 100 μA is recommended to avoid latch-up problems.
5. Static Sensitive Device. Unused devices must be stored in conductive material to protect devices from possible static damage.
6. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Theory of Operation

Figure 1 shows the major elements of the TSC7650A. There are two amplifiers, the main amplifier and the nulling amplifier; both have offset-null capability. The main amplifier is connected full-time from the input to the output. The nulling amplifier, under the control of the chopping frequency oscillator and clock circuit, alternately nulls itself and the main amplifier. Two external capacitors provide the required storage of the nulling potentials and the necessary nulling-loop time constants. The nulling arrangement operates over the full common-mode and power-supply ranges, and is also independent of the output level, thus giving exceptionally high CMRR, PSRR, and $A_{VOL}$.

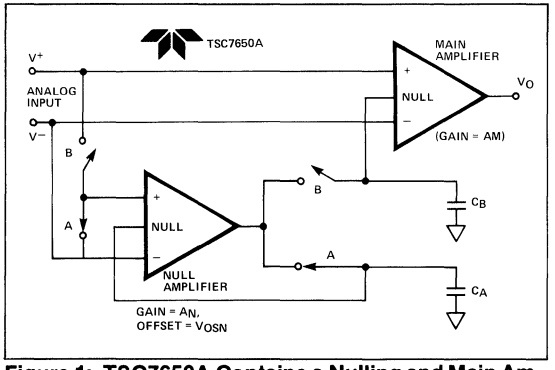


**Figure 1: TSC7650A Contains a Nulling and Main Amplifier. Offset Correction Voltages are Stored on Two External Capacitors.**

Careful balancing of the input switches minimizes chopper frequency charge injection at the input terminals, and the feed forward-type injection into the compensation capacitor that can cause output spikes in this type of circuit.

The circuits offset voltage compensation is easily shown. With the nulling inputs shorted a voltage almost identical to the nulling amplifier offset voltage is stored on $C_A$. The effective offset voltage at the null amplifier input is:

$$(1)\quad V_{OSE} = \frac{1}{A_N + 1} V_{OSN}$$

After the nulling amplifier is zeroed the main amplifier is zeroed; the A switches open and B switches close.

The output voltage equation is:

$$(2)\quad V_O = A_M \left[ V_{OSM} + (V^+ - V^-) + A_N(V^+ - V^-) + A_N V_{OSE} \right]$$

Substituting (1) → (2) and assuming $A_N >> 1$.

$$(3)\quad V_O = A_M A_N \left[ (V^+ - V^-) + \frac{V_{OSM} + V_{OSN}}{A_N} \right]$$

As desired the device offset voltages are reduced by the high open-loop gain of the nulling amplifier.

## Output Stage/Load Driving

The output circuit is a high-impedance stage (approximately 18 kΩ). With loads less than this the chopper amplifier behaves in some ways like a transconductance amplifier whose open-loop gain is proportional to load resistance. For example, the open-loop gain will be 17 dB lower with a 1 kΩ load than with a 10 kΩ load. If the amplifier is used strictly for dc the lower gain is of little consequence since the dc gain is typically greater than 120 dB even with a 1 kΩ load. In wideband applications, the best frequency response will be achieved with a load resistor of 10 kΩ or higher. This will result in a smooth 6 dB/octave response from 0.1 Hz to 2 MHz, with phase shifts of less than 10° in the transition region where the main amplifier takes over from the null amplifier. The clock frequency sets the transition region.

## Intermodulation

Previous chopper-stabilized amplifiers have suffered from intermodulation effects between the chopper frequency and input signals. These arise because the finite ac gain of the amplifier results in a small ac signal at the input. This is seen by the zeroing circuit as an error signal, which is chopped and fed back, thus injecting sum and difference frequencies and causing disturbances to the gain and phase vs. frequency characteristics near the chopping frequency. These effects are substantially reduced in the TSC7650A by feeding the nulling circuit with a dynamic current, corresponding to the compensation capacitor current, in such a way as to cancel that portion of the input signal due to a finite ac gain. The intermodulation and gain/phase disturbances are held to very low values, and can generally be ignored.

## Nulling Capacitor Connection

The offset voltage correction capacitors are connected to $C_A$ and $C_B$. The common capacitor connection is made to $V_S^-$ (Pin 4) on the 8-pin packages and to capacitor return ($C_R$, Pin 8) on the 14-pin packages. The common connection should be made through either a separate pc trace or wire to avoid voltage drops. The capacitors outside foil, if possible, should be connected to $C_R$ or $V_S^-$.

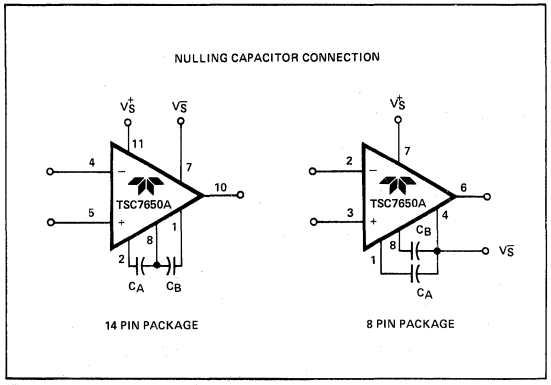


**Figure 2: Nulling Capacitor Connection**

## Clock Operation

The internal oscillator is set for a 300 Hz nominal chopping frequency on both the 8 and 14-pin dual in line packages. With the 14-pin DIP TSC7650A, the 300 Hz internal chopping frequency is available at the internal clock output (Pin 12). A 600 Hz nominal signal will be present at the external clock input pin (Pin 13) with EXT/INT high or open. This is the internal clock signal before a divide by two operation.

The 14-pin DIP device can be driven by an external clock. The INT/EXT input (Pin 14) has an internal pull-up and may be left open for internal clock operation. If an external clock is used INT/EXT must be tied to $V_S^-$ (Pin 7) to disable the internal clock. The external clock signal is applied to the external clock input (Pin 13).

The external clock amplitude should swing between $V_S^+$ and ground for power supplies up to ± 6 V and between $V^+$ and $V^+$ -6 V for higher supply voltages.

At low frequencies the external clock duty cycle is not critical since an internal divide by two gives the desired 50% switching duty cycle. The offset storage correction capacitors are charged only when the external clock input is high. A 50-80% external clock positive duty cycle is desired for frequencies above 500 Hz to guarantee transients settle before the internal switches open.

The external clock input can also be used as a strobe input. If a strobe signal is connected at the external clock input so that it is low during the time an overload signal is applied, neither capacitor will be charged. The leakage currents at the capacitor pins are very low. At 25° C a typical TSC7650A will drift less than 10 μV/sec.

## Output Clamp

Chopper-stabilized systems can show long recovery times from overloads. If the output is driven to either supply rail, output saturation occurs. The inputs are no longer held at a "virtual ground." The $V_{OS}$ null circuit treats the differential signal as an offset and tries to correct it by charging the external capacitors. The nulling circuit also saturates. Once the input signal returns to normal, the response time is lengthened by the long recovery time of the nulling amplifier and external capacitors.

Through an external clamp connection, the TSC7650A eliminates the overload recovery problem by reducing the feedback network gain before the output voltage reaches either supply rail.

The output clamp circuit is shown in Figure 3 with typical inverting and non-inverting circuit connections shown in Figure 4 and 5. Output voltage vs clamp circuit current characteristics are shown in the typical operating curves. For the clamp to be fully effective, the impedance across the clamp output should be greater than 100 kΩ.

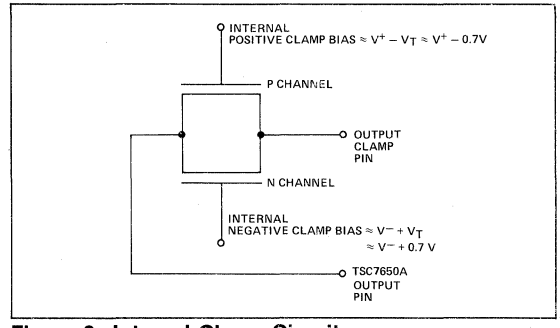


**Figure 3: Internal Clamp Circuit**

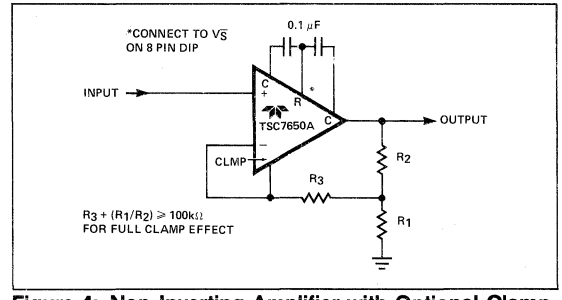


**Figure 4: Non-Inverting Amplifier with Optional Clamp**

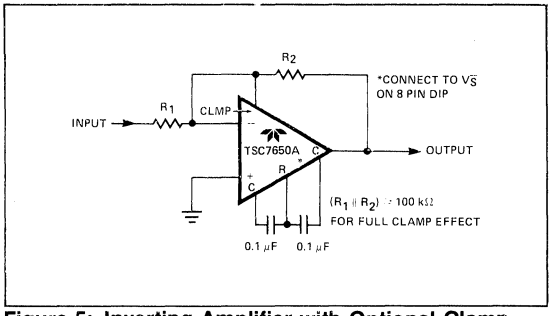


**Figure 5: Inverting Amplifier with Optional Clamp**

## Static Protection

All device pins are static-protected. Strong static fields and discharges should be avoided, however, as they can degrade diode junction characteristics and increase input-leakage currents.

Many companies are actively involved in providing services, educational material, and supplies to aid electronic manufacturers in establishing "static safe" work areas where CMOS components are handled. A partial company listing is:

- 3M
  Static Control Systems Division
  223-25W EM Center
  St. Paul, MN 55101
  (800) 792-1072
- Semtronics
  P.O. Box 592
  Martinsville, NJ 08836
  (210) 561-9520
- American Convertors
  1919 South Butlerfield Road
  Mundelein, IL 60060
  (312) 362-9000
- ACL
  1960 East Devon Avenue
  Elk Grove Village, IL 60007
  (312) 981-9212

## Latch-Up Avoidance

Junction-isolated CMOS circuits inherently include a parasitic 4-layer (p-n-p-n) structure which has characteristics similar to an SCR. Under certain circumstances this junction may be triggered into a low impedance state, resulting in excessive supply current. To avoid the condition, no voltage greater than 0.3 V beyond the supply rails should be applied to any pin. In general, the amplifier supplies must be established either at the same time or before any input signals are applied. If this is not possible, the drive circuits must limit input current flow to under 0.1 mA to avoid latchup.

## Thermo-Electric Potentials

Precision dc measurements are ultimately limited by thermoelectric potentials developed in thermocouple junctions of dissimilar metals, alloys, silicon, etc. Unless all junctions are at the same temperature, thermoelectric voltages typically around 0.1 μV/° C, but up to tens of μV/° C for some materials, will be generated. In order to realize the benefits extremely low offset voltages provide, it is essential to take special precautions to avoid temperature gradients. All components should be enclosed to eliminate air movement, especially those caused by power-dissipating elements in the system. Low thermoelectric-coefficient connections should be used where possible and power supply voltages and power dissipation should be kept to a minimum. High-impedance loads are preferable, and separation from surrounding heat-dissipating elements is advised.

## Pin Compatibility

On the 8-pin mini-dip TSC7650A the external null storage capacitors are connected to pins 1 and 8. On most other operational amplifiers these are left open or are used for offset potentiometer or compensation capacitor connections.

For OP05 and OP07 operational amplifiers, the replacement of the offset null pot between pins 1 and 8 by two capacitors from the pins to $V_S^-$ will convert the OP05/07 pin configuration for TSC7650A operation. For LM108 devices the compensation capacitor is replaced by the external nulling capacitors. The LM101/748/709 pin outs are modified similarly by also removing any circuit connections to pin 5. On the TSC7650A pin 5 is the output clamp connection. Other operational amplifiers may use this pin as an offset or compensation point.

The minor modifications needed to retrofit a TSC7650A into existing sockets operating at reduced power supply voltages make prototyping and circuit verification straight forward.

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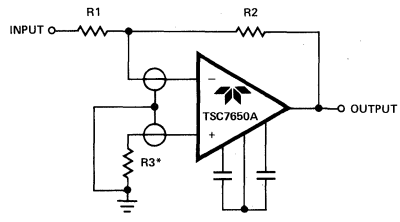
## Input Guarding

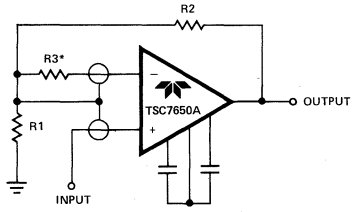
High impedance, low leakage CMOS inputs allow the TSC7650A to make measurements of high impedance sources. Stray leakage paths can increase input currents and decrease input resistance unless inputs are guarded. A guard is a conductive pc trace surrounding the input terminals. The ring connects to a low impedance point as the same potential as the inputs. Stray leakages are absorbed by the low impedance ring. The equal potential between ring and inputs prevents input leakage currents. Typical guard connections are shown in Figure 6.

The 14-pin DIP configuration has been specifically designed to ease input guarding. The pins adjacent to the inputs are unused.

In applications requiring low leakage currents, boards should be cleaned thoroughly and blown dry after soldering. Protective coatings will prevent future board contamination.




Inverting



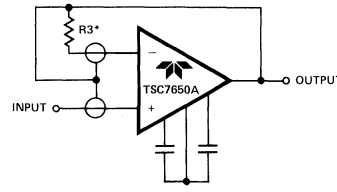

NOTE: $R_3 = \frac{R_1 R_2}{R_1 + R_2}$

Non-Inverting

*USE R3 TO COMPENSATE FOR LARGE SOURCE RESISTANCES, OR FOR CLAMP OPERATION.

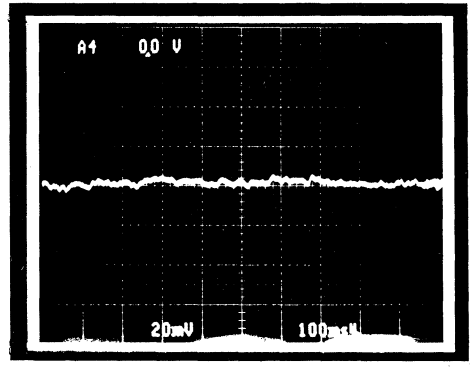
## Component Selection

The two required capacitors, $C_A$ $C_B$, have optimum values depending on the clock or chopping frequency. For the preset internal clock, the correct value is 0.1 μF. To maintain the same relationship between the chopping frequency and the nulling time constant, the capacitor values should be scaled in proportion to the external clock if used. High-quality film-type capacitors such as mylar are preferred. Ceramic or other lower-grade capacitors may be suitable in some applications. For fast settling on initial turn-on, low dielectric absorption capacitors (such as polypropylene) should be used. With ceramic capacitors, several seconds may be required to settle to 1 μV.




Follower

**Figure 6: Input Guard Connection**

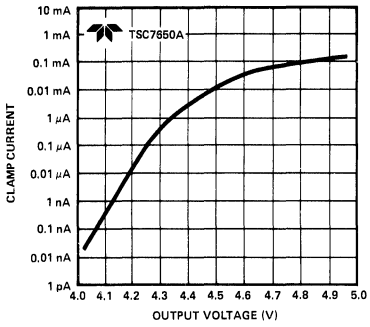



Gain = 1000, 1 Div = 20 $\mu V_{p-p}$

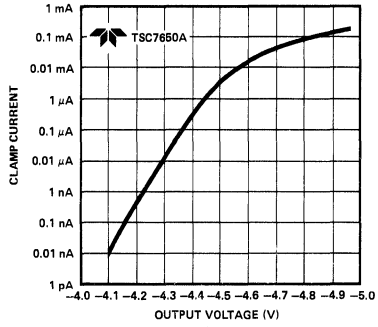
**Figure 7: TSC7650A Peak to Peak Noise (0.1 to 10Hz)**

## Typical Characteristic Curves

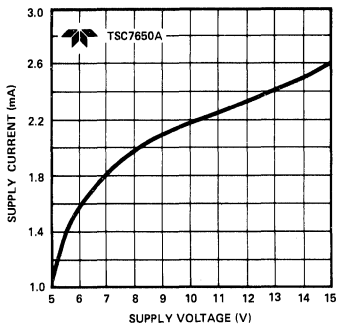
### Positive Clamp Current vs Output Voltage



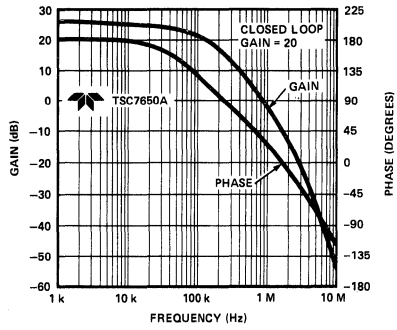

### Negative Clamp Current vs Output Voltage




### Supply Current vs Supply Voltage




### Gain/Phase vs Frequency

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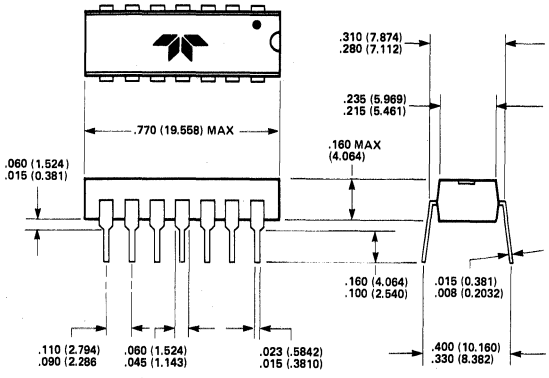
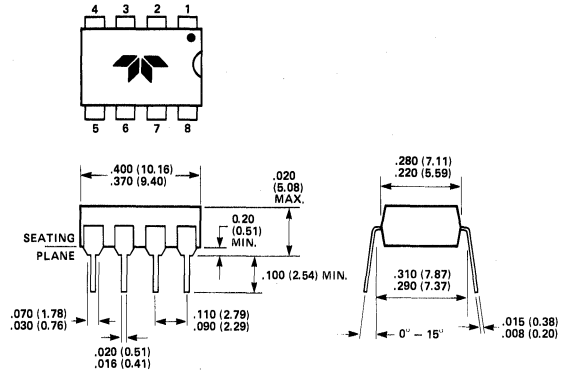
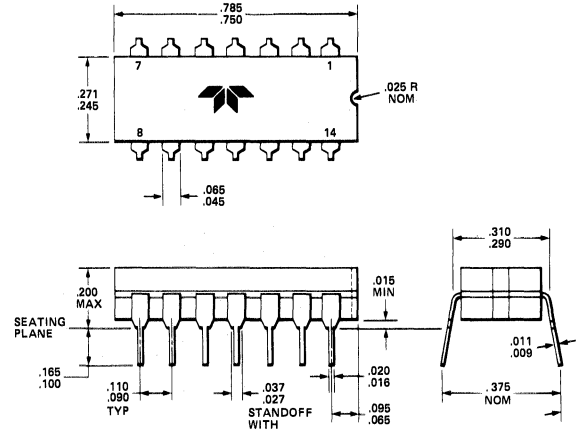
## Package Outline



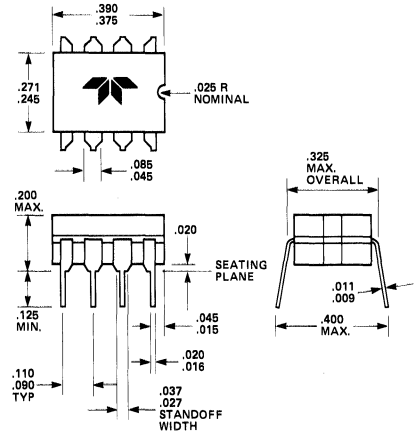

**14-Pin Plastic Package**
**(Package #6)**




**8-Pin Plastic Package**
**(Package #4)**




**14-Pin CerDIP Package**
**(Package #7)**




**8-Pin CerDIP Package**
**(Package #5)**